REMARKS

In response to the Office Action mailed September 9, 2004, Applicants respectfully request reconsideration.

The Office Action acknowledges Applicants' claim for priority. However, the Office Action states that Applicants have not filed a certified copy of the priority application. Applicants would like to point out that a copy of the priority document was filed on April 29, 2002. A copy of the return postcard, transmittal letter and copies of the first three pages of the priority document are enclosed that demonstrate that Applicants did in fact file the required certified copy of European application no. 01301092.1. Therefore, Applicants respectfully request that the next action in the application confirm receipt of the priority document and that the requirements for perfecting the priority claim pursuant to 35 U.S.C. §119 have been satisfied.

Claims 4, 5, 8, 9, 16, 17, 20, and 21 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite. The Office Action points to a number of antecedent basis issues in the claims. In response to this rejection, Applicants have amended the claims to overcome all of the noted deficiencies and believes that the claims are now clear enough to satisfy the statute.

The Office Action also objected to the Summary of the Invention. In response to this objection, Applicants have rewritten the Summary of the Invention so that the subject matter of the invention is described in one or more clear, concise sentences or paragraphs. Accordingly, Applicants believe this objection has been overcome and respectfully requests its withdrawal.

Claims 1-3, 6, 7, 13, 14, 18, and 25 were rejected under 35 U.S.C. §102(b) as being anticipated by Heybruck. Applicants respectfully traverse this rejection.

Heybruck describes apparatus for testing a field programmable logic gate array, in which an input multiplexer 22 can select between a functional input and pseudo random program generator (PRPG) input. The output of the input multiplexer is then passed to the input register which is then passed to the circuit element under test. Similarly the circuit under test outputs a result value to the output register and also to a multiple input signature register (MISR). The outputs of both the output register and the MISR are input to an output multiplexer which selects either the output from the output register or the MISR to the output. The input register 23 is

positioned between the output of the input multiplexer and the circuitry and therefore cannot supply the PRPG with an input.

By contrast, claim 1 recites test circuitry for testing an integrated circuit, the integrated being configurable to accept input data from stimulus scan cells and to provide output data to response scan cells. The test circuitry including stimulus circuitry for providing test data to the integrated circuit; input selection means operable to control which of the test data and the input data are received at the integrated circuit; capture circuitry for capturing output data from the integrated circuit and generating response data; output selection means operable to select which of the output data and the response data are received by the response scan cells. Clearly, Heybruck does not teach or suggest that the integrated circuit is configurable to accept input data from stimulus scan cells and to provide output data to response scan cells as recited in claim 1. Accordingly, claim 1 distinguishes over Heybruck and is in allowable condition.

Claims 2-10 depend from claim 1 and are allowable for at least the same reasons.

Claim 13 recites a method of testing an integrated circuit using test circuitry associated therewith, the test circuitry including stimulus circuitry; input selection means; capture circuitry; and output selection means; the integrated circuit being configurable to accept input data from stimulus scan cells and to provide output data to response scan cells, the method including the steps of: providing test data to the integrated circuit from the stimulus circuitry; operating the input selection means to control which of the test data and the input data are received at the integrated circuit; capturing output data from the integrated circuit using the capture circuitry; generating response data based on the output data; operating the output selection means to select which of the output data and the response data are received by the response scan cells. As discussed above in connection with claim 1, Heybruck does not teach or suggest at least the integrated circuit being configurable to accept input data from stimulus scan cells and to provide output data to response scan cells. Accordingly, claim 13 distinguishes over Heybruck and is in allowable condition.

Claims 14-22 depend from claim 13 and are allowable for at least the same reasons.

Claim 25 recites test circuitry for testing an integrated circuit, the integrated circuit being configurable to accept input data from stimulus scan cells and to provide output data to response

scan cells, the test circuitry including: stimulus circuitry for providing test data to the integrated circuit; input circuitry operable to control which of the test data and the input data are received at the integrated circuit; capture circuitry for capturing output data from the integrated circuit and generating response data; output circuitry operable to select which of the output data and the response data are received by the response scan cells. As discussed above in connection with claim 1, Heybruck does not teach or suggest at least the integrated circuit being configurable to accept input data from stimulus scan cells and to provide output data to response scan cells. Accordingly, claim 25 distinguishes over Heybruck and is in allowable condition.

Claims 11, 12, 23, and 24 were rejected under 35 U.S.C. §102(e) as being anticipated by Ngo et al. Applicants respectfully disagree with this rejection.

Ngo describes apparatus for performing programmable built in self testing of memory wherein, rather than saving all data subsequent to a first section of a memory failure, only a single memory block of data values is saved.

By contrast, claim 11 recites test circuitry for testing an integrated circuit, the test circuitry including stimulus circuitry and capture circuitry, the stimulus circuitry including a dictionary storing a plurality of read/write operation primitives, the primitives being combinable to form at least a first read/write testing sequence; and a librarian sub-block for receiving the input data, the input data being indicative of a test to be applied to the integrated circuit, the librarian sub-block being configured to control, on the basis of the input data, which of the primitives are provided to the integrated circuit, and the order in which they are provided, based on the input data; wherein the capture circuitry captures response data from the integrated circuit.

Although Ngo describes the use of an instruction register for storing instructions to be carried out to test the memory and a program counter which points to a specific element within the instruction register, this is not a dictionary storing a plurality of read/write operation primitives, the primitives being combinable to form at least a first read/write testing sequence and a librarian sub-block for receiving the input data the input data being indicative of a test to be applied to the integrated circuit. Accordingly, claim 11 distinguishes over Ngo and is in allowable condition.

Claim 12 depends from claim 11 and is allowable for at least the same reasons.

Claim 23 recites a method for testing an integrated circuit using test circuitry, the test circuitry including stimulus circuitry and capture circuitry, the stimulus circuitry including: a dictionary storing a plurality of read/write operation primitives, the primitives being combinable to form at least a first read/write testing sequence; and a librarian sub-block; the method including the steps of: receiving input data at the librarian sub-block, the input data being indicative of a test to be applied to the integrated circuit; selecting, on the basis of the input data and using the librarian sub-block, one or more of the primitives and an order of the primitives so selected; providing the selected primitives to the integrated circuit in the selected order; and capturing response data from the integrated circuit using the capture circuitry. As discussed above in connection with claim 11, Ngo does not teach or suggest a dictionary storing a plurality of read/write operation primitives, the primitives being combinable to form at least a first read/write testing sequence and receiving input data at the librarian sub-block, the input data being indicative of a test to be applied to the integrated circuit. Accordingly, claim 23 distinguishes over Ngo and is in allowable condition.

Claim 24 depends from claim 23 and is allowable for at least the same reasons.

CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,

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By: _____

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Docket No.: S1022.80845US00
Date: February 9, 2005
x02/09/05x

Serial No. 10/068 307 File No. S01022/80845 By: JHM

Title: Built-In Test Support for an Integrated Circuit

Application of Steven Curtis et al. WGS Date: 5-7-02

The U.S. PTO Mail Room acknowledges receipt of the following on the date stamped hereon:

[ ] Mailing by Express Mail (37 CFR 1.10)
Express Mail Label No. _____
[ ] Patent Application
[ ] Non-provisional [ ] Provisional
Incl. _____ pages, (pgs) Specification,
(pgs) Abstract, (pgs) Claims (_____ # claims)
[ ] Design Patent Application
[X] Declaration(s)
[X] Drawings 3 Sheet(s) (FIGS. 1 - 4)
[X] Formal [ ] Informal
[ ] Utility Patent Application Transmittal
[ ] Fee calculation sheet (x2)
[ ] CPA Transmittal
[ ] Verified Statement claiming small entity status
[ ] Assignment and Cover Sheet

[ ] Provisional Application Cover Sheet
[ ] Multiple Dependent Claim Fee Sheet
[X] Inf. Discl. Statement, PTO Form 1449
[X] References Cited
[X] Priority Document(s) # 01301092.1
[X] Copy of Notice to File Missing Parts
[ ] Amendment/Response
[ ] Petition for Ext. of Time (x2)
[ ] Issue Fee Transmittal
[ ] Letter to Official Draftsperson
[ ] Notice of Appeal
[ ] Brief (x3)
[X] Check for $ 1128 Check # _____
[X] Transmittal Letter (x2)
[X] Cert. of Mailing under 37 CFR 1.8(a)

[ ] Other _____

DATE MAILED 4-29-02

Attorney's Docket No. S01022/80845

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Steven FIRTH and William Bryan BARNES
Serial No.: 10/068,307
Filing Date: February 6, 2002
For: BUILT-IN TEST SUPPORT FOR AN INTEGRATED CIRCUIT

Examiner: Unassigned
Art Unit: 2858

Box Missing Parts
Commissioner for Patents
Washington, D.C. 20231

Sir/Madam:

Transmitted herewith for filing is/are the following document(s):

[X] Notice to File Missing Parts
[X] Declaration and Power of Attorney
[X] 3 Sheets of Formal Drawings
[X] Information Disclosure Statement, PTO Form 1449 and Cited References
[X] Certified Copy of European Priority Application No. 01301092.1
[X] Return Post Card

If the enclosed papers are considered incomplete, the Mail Room and/or the Application Branch is respectfully requested to contact the undersigned collect at (617)720-3500, Boston, Massachusetts.

The enclosed check includes a $740.00 filing fee, $130.00 surcharge and $258.00 additional claim fee for a total of $1,128.00. If the fee is insufficient, the balance may be charged to the account of the undersigned, Deposit Account No. 23/2825. A duplicate of this sheet is enclosed.

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

I hereby certify that this document is being placed in the United States mail with first-class postage attached, addressed to the Commissioner for Patents, Washington, D.C. 20231 on April 29, 2002.

Respectfully submitted,

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Attorney Docket No.: S01022/80845
X05/07/02

Europäisches Patentamt | European Patent Office | Office européen des brevets

Bescheinigung | Certificate | Attestation

Die angehefteten Unterlagen stimmen mit der ursprünglich eingereichten Fassung der auf dem nächsten Blatt bezeichneten europäischen Patentanmeldung überein.

The attached documents are exact copies of the European patent application described on the following page, as originally filed.

Les documents fixés à cette attestation sont conformes à la version initialement déposée de la demande de brevet européen spécifiée à la page suivante.

Patentanmeldung Nr. | Patent application No. | Demande de brevet n°

01301092.1

Der Präsident des Europäischen Patentamts;
Im Auftrag

For the President of the European Patent Office

Le Président de l'Office européen des brevets
p.o.

R C van Dijk

DEN HAAG, DEN
THE HAGUE, 08/02/02
LA HAYE, LE

Europäisches Patentamt
European Patent Office
Office européen des brevets

Blatt 2 der Bescheinigung
Sheet 2 of the certificate
Page 2 de l'attestation

Anmeldung Nr.:
Application no.:
Demande n°: 01301092.1

Anmeldetag:
Date of filing:
Date de dépôt: 07/02/01

Anmelder:
Applicant(s):
Demandeur(s):
STMicroelectronics Limited
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UNITED KINGDOM

Bezeichnung der Erfindung:
Title of the invention:
Titre de l'invention:
Built-in test circuit and method for an integrated circuit

In Anspruch genommene Priorität(en) / Priority(ies) claimed / Priorité(s) revendiquée(s)

Staat: State: Pays:	Tag: Date: Date:	Aktenzeichen: File no. Numéro de dépôt:

Internationale Patentklassifikation:
International Patent classification:
Classification internationale des brevets:
G11C29/00

Am Anmeldetag benannte Vertragstaaten:
Contracting states designated at date of filing: AT/BE/CH/CY/DE/DK/ES/FI/FR/GB/GR/IE/IT/LI/LU/MC/NL/PT/SE/TR
Etats contractants désignés lors du depôt:

Bemerkungen:
Remarks:
Remarques:

BUILT-IN TEST SUPPORT FOR AN INTEGRATED CIRCUIT

FIELD OF INVENTION

The present invention relates to testing of integrated circuits using built-in testing circuitry.

The invention has been developed primarily for use in testing memory circuitry, and will be described hereinafter with reference to this application. However, it will be appreciated that the invention is not limited to this particular use and can be applied to many other types of integrated circuits having scan chains for data input and output.

BACKGROUND TO INVENTION

Presently, memory testing at integrated circuit level is usually handled in one of two ways. For relatively small memories (say, about 500 bytes or less), existing scan chains can be used. For example, referring to Figure 1, data is fed serially into stimulus scan cells 10 until they contain the desired input values. The output of the stimulus scan cells 10 is then clocked into a memory location within memory block 11. The memory location is read out into response scan cells 12, and the output is compared with that the original input. This can be done using, for example, a comparator (not shown).

There are a number of standard test data sequences that are used within field of memory testing. These tests are called Marinescu XN tests, where X represents the number of read/write